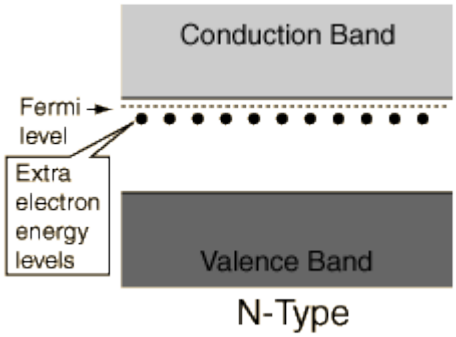
PHSACOR10T - Analog Systems and Applications (AFTER REDUCTION)

Semiconductor Diodes **5 Lectures**

P and N type semiconductors. Energy Level Diagram. Conductivity and Mobility, Concept of Drift velocity. Barrier Formation in PN Junction Diode. Static and Dynamic Resistance. Current Flow Mechanism in Forward and Reverse Biased Diode.

N-Type Band Structure

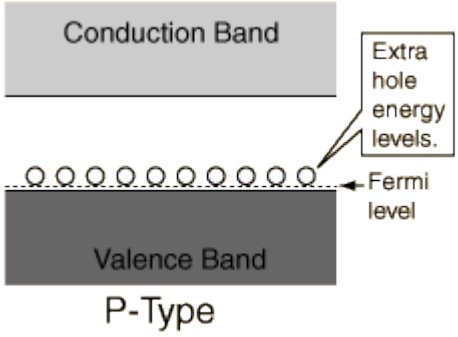
The addition of donor impurities contributes electron energy levels high in the semiconductor band gap so that electrons can be easily excited into the conduction band. This shifts the effective Fermi level to a point about halfway between the donor levels and the conduction band.



Electrons can be elevated to the conduction band with the energy provided by an applied voltage and move through the material. The electrons are said to be the "majority carriers" for current flow in an n-type semiconductor.

P-Type Band Structure

The addition of acceptor impurities contributes hole levels low in the semiconductor band gap so that electrons can be easily excited from the valence band into these levels, leaving mobile holes in the valence band. This shifts the effective Fermi level to a point about halfway between the acceptor levels and the valence band.



Electrons can be elevated from the valence band to the holes in the band gap with the energy provided by an applied voltage. Since electrons can be exchanged between the holes, the holes are said to be mobile. The holes are said to be the "majority carriers" for current flow in a p-type semiconductor.

Electrical conductivity and mobility

The electrical conductivity of intrinsic semiconductors in the not very low temperature range is due to intrinsic charge carriers, that is due to electrons and holes. Such conductivity is sometimes termed as intrinsic conductivity.

There are two types of carriers in the intrinsic semiconductor. So it's specific conductance is the sum of the conductivity $\boldsymbol{\sigma_n = |e|n\mu_n}$ due to free electron with concentration n and mobility μ_n and of the conductivity $\sigma_p = |e|p\mu_p$ due to presence of holes, with the concentration p and mobility μ_p.

The mobility is the magnitude of the velocity but unit electric field. $\mu = \frac{v_d}{E}$

The mobility is defined to be positive for both electrons and holes, although their drift velocities are opposite. In an ideal semiconductor the mobility is determined by the collision between electrons and phonons.

The electrical conductivity of a semiconductor is $\boldsymbol{\sigma = |e|n\mu_n + |e|p\mu_p}$

Since for an intrinsic semiconductor $n = p = n_i$ then $\boldsymbol{\sigma_i = |e|n_i(\mu_n + \mu_p)}$.

Here σ_i denotes that intrinsic conductivity.

Conductivity is proportional to the product of mobility and carrier concentration.

For example, the same conductivity could come from a small number of electrons with high mobility for each, or a large number of electrons with a small mobility for each. For metals, it would not typically matter which of these is the case, since most metal electrical behaviour depends on conductivity alone. Therefore, mobility is relatively unimportant in metal physics.

On the other hand, for semiconductors, the behaviour of transistors and other devices can be very different depending ***on whether there are many electrons with low mobility or few electrons with high mobility.*** Therefore, mobility is a very important parameter for semiconductor materials. Almost always, higher mobility leads to better device performance,

with other things equal. Semiconductor mobility depends on the impurity concentrations (including donor and acceptor concentrations), defect concentration, temperature, and electron and hole concentrations. It also depends on the electric field, particularly at high fields when velocity saturation occurs. It can be determined by the Hall effect, or inferred from transistor behaviour.

What is Drift Velocity?

Subatomic particles like electrons move in random directions all the time. When electrons are subjected to an electric field they do move randomly but they slowly drift in one direction, in the direction of the electric field applied. The net velocity at which these electrons drift is known as drift velocity. Drift velocity can be defined as: **The average velocity attained by charged particles, (eg. electrons) in a material due to an electric field.**

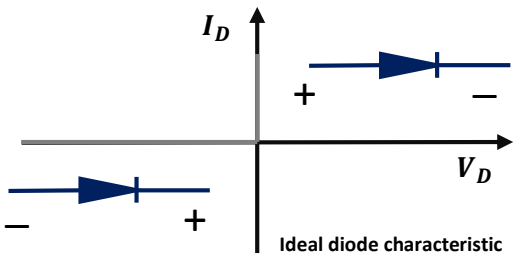
Ideal PN junction diode, I-V characteristics

When one side of a single crystal of a semiconductor is doped with donor impurity atoms (diffused impurities with five valance electrons) and the other side of the same crystal with acceptor impurity (diffused impurity with three valance electrons) a p-n junction is formed.

It conducts well when a voltage is applied across the junction with some definite polarities, but it is non-conducting when a voltage is applied across the junction with opposite polarities. Thus it has properties similar to that of vacuum diode. For this a p-n junction is called a semiconductor diode.

Simple by joining a p-type material to an n-type material a p-n junction with useful electrical properties cannot be formed because in this case lattice structure remains discontinuous at the junction. Thus the fabrication of p-n junction requires a highly develop semiconductor technology.

Ideal Diode: Ideally, a diode will conduct current in the direction defined by the arrow in the symbol and act like an open circuit to establish current in opposite direction. In essence: the characteristics of an ideal are those of a switch that can conduct current only one direction. The ideal diode therefore, is a short circuit for their region of conduction.



Real Diode: Practically no real diodes behave perfectly as said earlier diode is also an electronic component with asymmetric conductance; it has low (ideally zero) resistance to current in one direction and high (highly infinite) resistance in other direction. Now since diode is a two terminal device, the application of a voltage across is terminal leaves three possibilities: (i) **No bias** (V_D=0 volt); (ii) **Forward bias** ($V_D > 0$ volt); (iii) **Reversed bias** ($V_D < 0$ volt). Each is a condition that will result in a response that the user must clearly understand if the device is to be applied effectively.

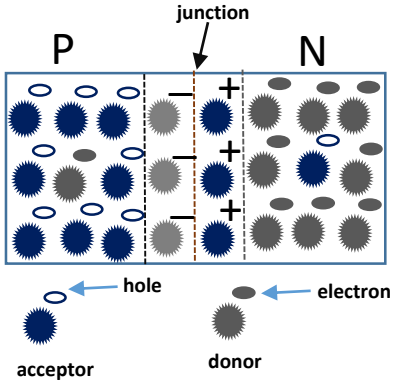
No bias or Open bias of a p-n junction:

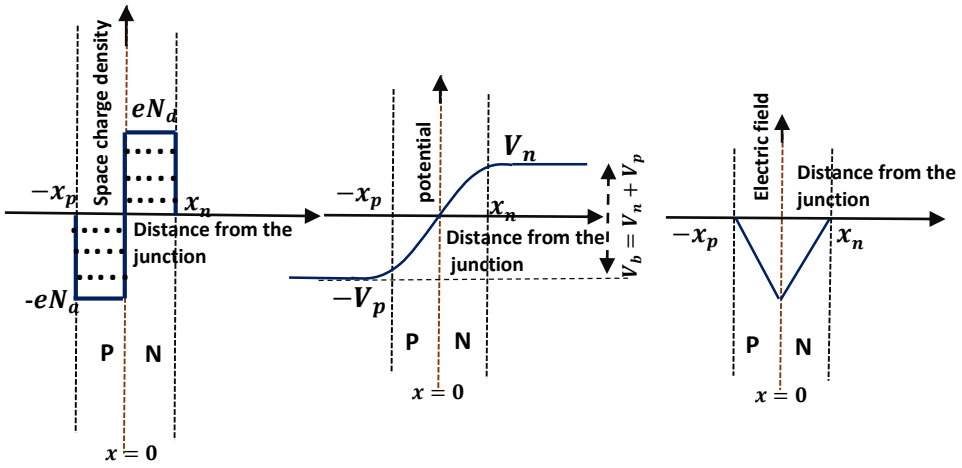
Because of difference in carrier concentration as soon as p-n junction is formed electrons from n-side diffuse from p-side and holes from p-side diffuse from n-side. The electrons from n-side after crossing the junction recombine with holes in p-side. Similarly, holes from p-side after crossing the junction recombine with free electrons in n-side. As a result, the region near the junction which depleted of mobile charges and contains only immobile ionic charges is called **Depletion region** or **space charge region** or **transition region**. The space charge, thus formed, develops an internal electrostatic potential barrier across the junction which tends to prevent further electron and hole diffusion. In equilibrium condition the internal potential barrier becomes high enough to restrain the process of diffusion.

** Note that, because of statistical distribution of velocities there are always a few majority holes which have enough energy to overcome the potential barrier and move from p-side to n-side. The magnitude of (this diffusion) current due flow of majority holes is governed by the

height of barrier. In equilibrium the potential barrier is assume as such a height that net current due to movement of holes become zero (As there are also always some minority holes in n-side, because of their random motion move close to the junction can immediately slide down the potential barrier).

Similarly, for electrons there will be two types of flow: Minority electrons from p-side to n-side and majority electrons from n-side to p-side. Again at equilibrium these two current counter balance each other and yield current. Thus in an open circuited p-n junction a condition of dynamical equilibrium is set.



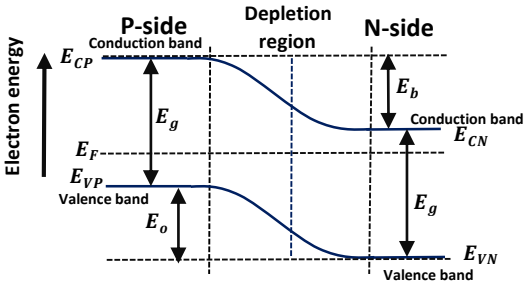


Q1. "The barrier potential across a p-n junction diode cannot be measure simply by placing a volt meter across the diode terminal"-explain.

To show a reading a small amount of current must flow through the circuit. It causes Joule heating in the circuit. Since there is no external source of energy it must causes simultaneous cooling of p-n junction which contradicts the principle of thermodynamics, according to which it is impossible to derive work by cooling a body below its equilibrium temp. Thus no current can pass through the circuit and voltmeter shows zero reading.

Actually the barrier potential is balanced by the metal-to-semiconductor contract potentials in the circuit.

Energy band diagram (open circuit): The positive space charge appears on the n-side of the junction and negative space charge on the p-side raise the position of all the energy levels including Fermi levels of the p-side and lower sit on the n-side.



In the energy band diagram we plot the energy of an electron which has a negative charge. Due to charge transfer p-side acquires a negative charge and for this p-bonds are slightly raised relative to the n- bonds. Clearly, in equilibrium condition bond edge E_{CP} in the p-side will be at higher level than the conduction band edge E_{CN} in the side. Similarly the valance band edge E_{VP} in the p-side will be higher level than the valance band edge E_{VN} in the n-side. Note that, electrostatic potential barrier

$$V_b = \frac{E_b}{e} = \frac{KT}{e} ln \frac{N_a N_d}{{n_i}^2}$$

Q2. On which factors does the height of potential barrier and width of the depletion region depend?

The internal potential barrier V_O across the junction is given by $V_O = \frac{KT}{e} ln \frac{N_a N_d}{{n_i}^2}$

[K =Boltzman constant, T =absolute temp. of the junction, N_a =no. of acceptor impurity atoms, N_d = no. of donor impurity atoms per unit volume, n_i =intrinsic carrier concentration (no. of electrons or holes per unit volume)]

Again the width X_n of the depletion region in the N-region and the width X_p in the P-region are given by $x_p = \sqrt{\frac{2\epsilon_r \epsilon_0 V_p}{eN_a}}$ and $x_n = \sqrt{\frac{2\epsilon_r \epsilon_0 V_n}{eN_d}}$

$$[where\ \epsilon_0 = free\ space\ permitivity\ \epsilon_r = dielectic\ constant\ of\ the\ water$$

[V_n =Magnitude of potential rise in the N region V_p =magnitude of potential fall in the P region]

Hence if N_a *or* N_d increase width of the depletion region in the p-side or n-side decreases.

Total width of the depletion region is $d = x_1 + x_2 = \sqrt{\frac{2\epsilon_r\epsilon_0 V_0}{e}\left(\frac{1}{N_a} + \frac{1}{N_d}\right)}$

[where$V_b = V_n + V_p$ =inernal potential barrier]

Hence value of the height of the potential barrier hence width of the depletion layer depends on the-

(i) The donor and acceptor impurity concentration on the both side of p-n junction.

(ii) Temperature.

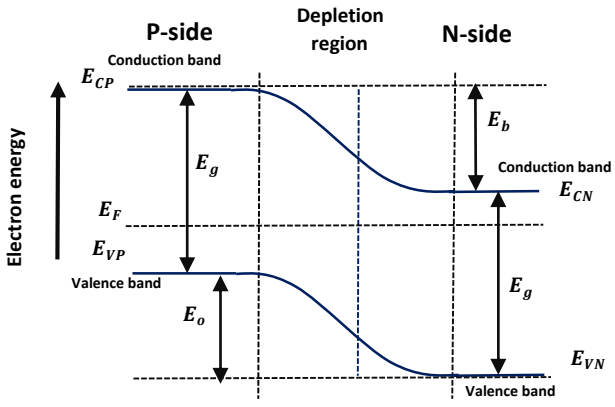
(iii) The nature of the semiconductor.

Q2. (a) Draw a Schematic diagram of the energy band diagram of an open circuited p-n junction.

(b) Draw a Schematic diagram of the energy band structure of F.B and R.B p-n junction.

(c) Explain its action as a rectifier from band diagram.

a)

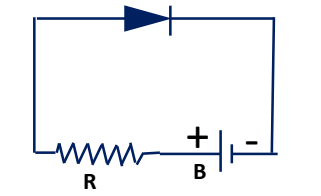


b) Forward Bias:

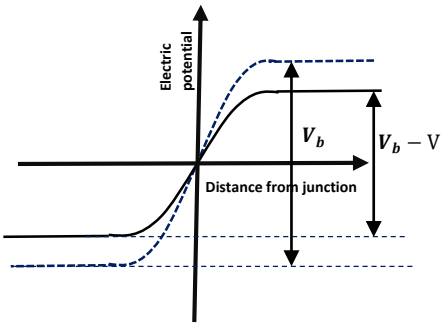
When the positive terminal of a battery is connected to the p-region and the negative terminal to the n-region, so that the potential difference acts in opposition to the internal potential barrier, the junction is said to be forward biased.

Under the forward bias condition, the applied positive potential repels the holes in the p-region towards the junction and the applied negative potential repels the electrons in the n-region also towards the junction. As a result, the positive donor ions and the negative acceptor ions within the depletion region regain electrons and holes respectively consequently the depletion region and the internal potential barrier disappears if applied potential difference is more than internal potential difference.

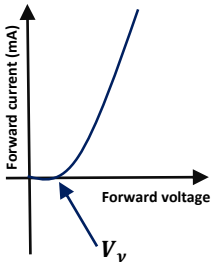
Therefore, under the action of the forward potential difference the majority carriers i.e. electron from n-region and holes from p-region flows across the junction, the number of electrons in the n-region always remain constant because the source of the external potential difference compensates for loss of electrons in the n-region (as electrons moves towards the positive terminal of the battery from crystal).



Forward biased P-N junction

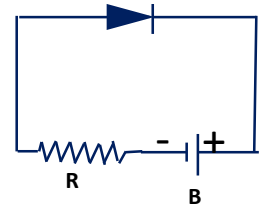


Forward bias reduced the potential

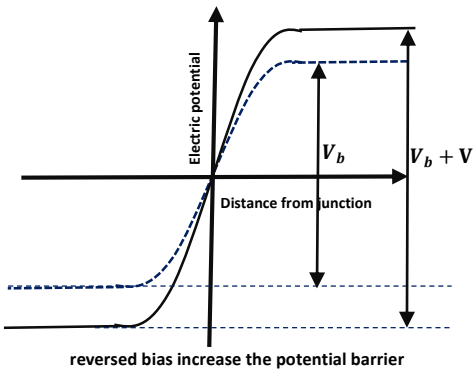


Reverse Bias:

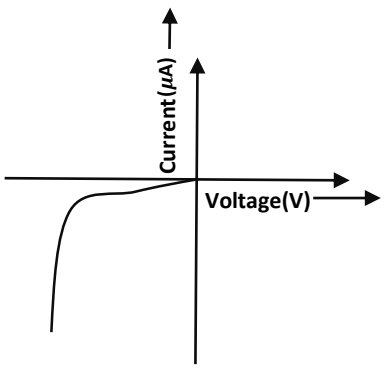
If the polarity of the applied voltage (V) is such that p-side becomes negative and n-side becomes positive, the height of the intrinsic potential barrier is increase to $V_b + V$. The junction is then said to be reverse biased. The increased barrier height makes the current due to flow of majority carriers negligible. Minority carriers moves down the potential barrier and hence their motion is not affected by the barrier height. They constitute a small current in the reverse direction, called reverse saturation current.



Reversed biased P-N junction



reversed bias increase the potential barrier



c) When a F.B voltage V is applied to the junction; the energy barrier is lowered to the value $(E_b - eV)$ as a result a good number of electrons from conduction band of n-side diffuse into p-side where they recombine with holes. This gives rise to a large component of diffusion current.

But when a R.B voltage V is applied to the junction, the energy barrier is raised to the value $(E_b + eV)$. Now very few electrons in the conduction band of n-side and holes in the valence band of p-side will have enough energy to surmount the increased barrier, hence diffusion current is negligibly small in a reverse bias. **This means that the junction can be used as a rectifying element to convert a.c into d.c.**

Q3. Write down the relationship between current and voltage in p-n junction diode, and explain the variation of current with voltage.

The current flowing through a p-n junction can be approximated by the relation,

$$I = I_0\left(e^{\frac{eV}{\eta kT}} - 1\right).....\text{(i)}$$

[Where I_0= reverse saturation current, V =applied voltage in volt, k =Boltzmann const., T=junction temp., e=charge of electron, η is a dimension less parameter having value between 1 & 2]

If the forward voltage V is large compared with $\frac{kT}{e}$ than the above relation can be written as $I = I_0 \exp\left(\frac{eV}{\eta kT}\right)$. This shows that forward current increases exponentially with applied voltage. For a reverse biased p-n junction V is negative.

$$I = I_0\left(e^{\frac{eV}{\eta kT}} - 1\right) = I_0\left(\frac{1}{e^{\frac{eV}{\eta kT}}} - 1\right).$$

If magnitude of V is very large compared with $\frac{kT}{e}$ the current $I \approx -I_0$.

Q4. Define cut in voltage.

In practical Si and Ge diodes it is found that the forward current does not assume significant value unless the forward biased exceeds certain threshold voltage V_v, called cut in voltage. The existence of V_v can be explained from the intrinsic potential barrier V_b existing across the junction. The current through the diode becomes applicable when the forward voltage exceeds V_b. Thus V_v is equal to the forward voltage for which the effective barrier vanishes. $V_v = 0 \cdot 2 - 0 \cdot 3 \; for \; Ge \; \& \; V_v = 0 \cdot 6 - 0 \cdot 7 \; for \; Si.$

Note that cut in voltage V_v depends upon doping concentration as well as temperature.

Q5. What do you mean by static and dynamical resistance of a diode? How does the dynamical resistance vary with current and temperature?

The ratio of applied voltage and to the current is known as static or d.c resistance of a diode is $r_{d.c} = \frac{V}{I}$.

If the resistance offered by the diode to flow of steady current. Since diode is non-linear device its d.c resistance varies with current. The resistance offered by the diode to the varying component of current is called dynamic or incremental resistance.

If is given by the reciprocal of the slope of current voltage characteristic curve at the operating point. Thus $r_{a.c} = \frac{dV}{dI}$.

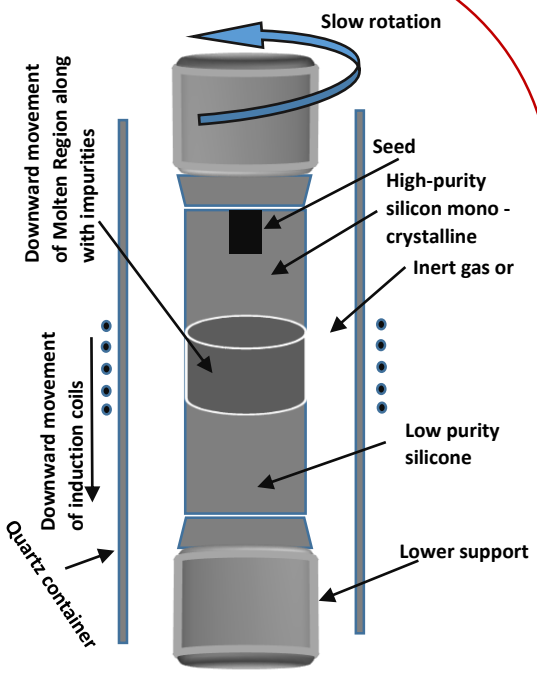
Now we have $I = I_0\left(e^{\frac{eV}{\eta kT}} - 1\right)$ then $\frac{dV}{dI} = \frac{e}{\eta kT} e^{\frac{eV}{\eta kT}}(I + I_0) \approx \frac{eI}{\eta kT}$ when $r_{a.c} = \frac{dV}{dI} = \frac{\eta kT}{eI}$

[kT/e=thermal voltage=$26mV$ room temp.]

As $k = 1.38 \times 10^{-23} J/K, e = 1.6 \times 10^{-9} c, T = 300K$ $\quad \therefore \boxed{r_{a.c} = \frac{26\eta}{I}}$

[Here I is in mA]

Fabrication techniques of a P-N junction diode (****)



In practice, the P-N junction is formed from a single mono crystalline structure by adding carefully controlled amounts of donor and acceptor impurities. Here discussion is limited only to acquaintances with the basic techniques and terminology (not expertise in fabrication).

The first and foremost requirement is to obtain an extremely pure germanium or silicon. Impurity of less than one-part in ten billion (10^{10}) is required for most semiconductor device fabrication to-day. For obtaining pure semiconductor material it is first purified chemically.

For reducing the impurities further, and to ensure the formation of a mono crystalline structure, a technique known as flatting zone is quite often employed. The mono crystalline structure is formed through the use of a small seed of semiconductor (e.g., silicon or germanium). The seed itself is a monocrystalline that has been very carefully cut along the face of its cubic lattice. Support clamps are employed to hold the low-purity polycrystalline rod. The rod, seed, and support clamps are placed in a quartz cylinder. The process may be carried out in vacuum or by surrounding the semiconductor with an inert gas. Great care is required to ensure that the semiconductor is not further contaminated during the floating zone process.

Induction coils encompass the quartz container, as shown in figure. The coils are excited by a radio-frequency voltage. Circulating currents are induced in the semiconductor due to the magnetic field set up by RF currents flowing through the induction coils. The heat so produced melts the zone which is exposed to it. As a result, a molten region is formed.

Slow rotation of rod makes the semiconductor atoms to align themselves with the atoms in the monocrystalline seed. Thus as the induction coils are moved downward, the molten region follows, and a monocrystalline structure continues to grow from the seed. Purification of the semiconductor rod occurs simultaneously with the formation of the mono-crystal. The impurities in the semiconductor rod tend to become 'more liquid' than the semiconductor. Thus as the induction coils are moved downward, the impurities tend to follow the molten region. Once the induction coils have traversed the length of the semiconductor rod, the impurities are collected in its lower end. The lower end of the semiconductor rod may then be cut off, and the process is repeated until the desired impurity level is attained.

Once a pure monocrystalline semiconductor has been produced, carefully controlled I amount of donor and acceptor impurities are added to the semiconductor without disturbing the orderly monocrystalline structure. Thus a P-N junction is formed.

Semiconductor diodes are normally one of the following types:

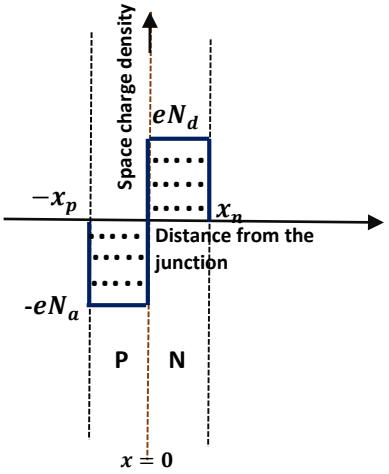
1. Grown junction diode
2. Alloy type or fused junction diode
3. Diffused junction diode
4. Epitaxial grown or planar diffused diode
5. Point contact diode

(****) It is not included in the revised syllabus

Derivation for Barrier Potential, Barrier Width and Current for Step Junction. (****)

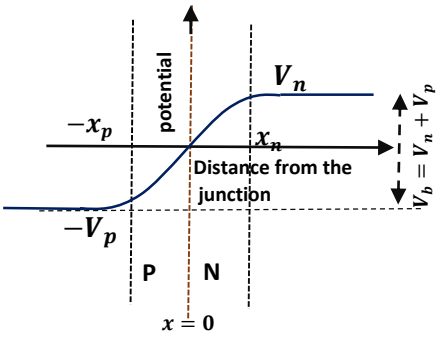
Height of potential barrier for Step Junction

In an open circuited PN junction net holes and net electron current must be zero separately.



Considering holes only $J_p = ep\mu_p E - eD_p \frac{dp}{dx} = 0$

μ_p = where holes mobility, p = the density of holes, E =applied electric field, e =magnitude of charge of an electron, D_p = diffusion coefficient, $\frac{dp}{dx}$ =concentration gradient of holes. Note that concentration gradient is negative as it is directed along negative x-axis.



Then $\frac{dp}{dx} = \frac{ep\mu_p E}{eD_p}$ or, $\frac{dp}{P} = \frac{\mu_p E}{D_p} dx = \frac{e}{kT} Edx$

or, $\frac{dp}{P} = -\frac{e}{kT} dV \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (i)$ [as $Edx = -dV$]

Integrating equation (i) from p region to n region $(-x_p \; to \; x_n \;)$

we get $ln\frac{p_n}{p_p} = -\frac{e}{kT}\left(V_p + V_n\right) = -\frac{e}{kT} V_b$ [where $V_b = V_n + V_p$ is the contact potential difference or potential barrier.]

And p_p & p_n represent the hole concentration in the P and N region respectively

Hence $\boxed{V_b = \frac{kT}{e} ln\frac{p_p}{p_n}} \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (ii)$ Hence $p_n = p_p e^{-\frac{e}{kT}V_b}$

Note that at moderate temperatures practically all the impurity atom is are ionised and the equilibrium concentration of holes in the P-side is $p_p = p_{p0} = N_a$

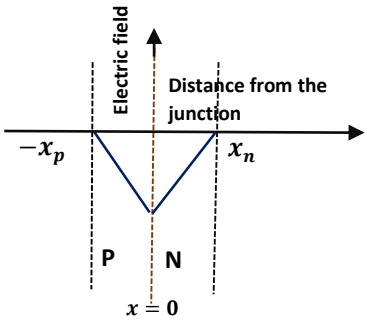
& $n_n = n_{n0} = N_d$ then from mass action law $p_n n_n = {n_i}^2$ then $p_n = \frac{{n_i}^2}{N_d} \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (iii)$

From equation (ii) and equation (iii) $\boxed{V_b = \frac{kT}{e} ln\frac{N_a N_d}{{n_i}^2}}$

Width of depletion region for Step Junction

From Poisson's equation in one dimension $\frac{d^2V}{dx^2} = \frac{eN_a}{\varepsilon}$ for $x < 0$

And $\frac{d^2V}{dx^2} = -\frac{eN_d}{\varepsilon}$ for $x > 0$



Integrating with get $\frac{dV}{dx} = \frac{eN_a}{\varepsilon}x + C_1$ and $\frac{dV}{dx} = -\frac{eN_d}{\varepsilon}x + C_2$

[where symbols have their usual meanings]

Boundary condition $\frac{dV}{dx} = 0$ at $x = -x_p$ and at $x = x_n$

Then $C_1 = -\frac{eN_a}{\varepsilon}(-x_p) = \frac{eN_a}{\varepsilon}x_p$ and $C_2 = \frac{eN_d}{\varepsilon}x_n$

Hence $\frac{dV}{dx} = \frac{eN_a}{\varepsilon}(x + x_p) \ldots\ldots(i)$ and $\frac{dV}{dx} = \frac{eN_d}{\varepsilon}(x_n - x) \ldots\ldots\ldots (ii)$

After integration we get $V = \frac{eN_a}{\varepsilon}\left(\frac{x^2}{2} + x_p x\right) + C_3$

and $V = \frac{eN_d}{\varepsilon}\left(x_n x - \frac{x^2}{2}\right) + C_4$

Boundary condition $V = -V_p$ at $x = -x_p$ and $V = V_n$ at $x = x_n$

Then $-V_p = \frac{eN_a}{\varepsilon}\left(\frac{(-x_p)^2}{2} + x_p(-x_p)\right) + C_3$ then $C_3 = -V_p + \frac{eN_a}{\varepsilon}\frac{{x_p}^2}{2}$

and similarly $C_4 = V_n - \frac{eN_d}{\varepsilon}\frac{{x_n}^2}{2}$

Then $V = -V_p + \frac{eN_a}{\varepsilon}\frac{(x_p+x)^2}{2} \ldots\ldots(iii)$ and $V = V_n - \frac{eN_d}{\varepsilon}\frac{(x_n-x)^2}{2} \ldots\ldots(iv)$

Now from third figure at $x = 0$ equation (i)& (ii) gives the same value of $\frac{dV}{dx}$.

Hence $\frac{eN_a}{\varepsilon}x_p = \frac{eN_d}{\varepsilon}x_n \ldots\ldots(v)$

From equation (v) we have $\frac{x_n}{x_n+x_p} = \frac{N_a}{N_a+N_d}$ or, $x_n = \frac{N_a}{N_a+N_d}(x_n + x_p) \ldots\ldots\ldots\ldots (vi)$

Again at $x = 0$ equation (iii)& (iv) gives the same value of V.

Hence $-V_p + \frac{eN_a}{\varepsilon}\frac{(x_p)^2}{2} = V_n - \frac{eN_d}{\varepsilon}\frac{(x_n)^2}{2}$

Or, $V_n + V_p = \frac{eN_a}{\varepsilon}\frac{(x_p)^2}{2} + \frac{eN_d}{\varepsilon}\frac{(x_n)^2}{2} = \frac{eN_d}{\varepsilon}\frac{x_n}{x_p}\frac{(x_p)^2}{2} + \frac{eN_d}{\varepsilon}\frac{(x_n)^2}{2}$

$\therefore V_b = \frac{eN_d}{2\,\varepsilon}x_n(x_p + x_n) = \frac{e}{2\,\varepsilon}\frac{N_dN_a}{(N_a+N_d)}(x_n + x_p)^2$

[using equation (vi) and where $V_b = V_n + V_p$]

Then width of the depletion layer is $W = x_n + x_p = \sqrt{\frac{2\varepsilon}{e}\,V_b\,\frac{(N_a+N_d)}{N_dN_a}}$

Hence $W = \sqrt{\frac{2\varepsilon KT}{e^2}\,ln\frac{N_aN_d}{{n_i}^2}\frac{(N_a+N_d)}{N_dN_a}}$

<u>Current for Step Junction.</u>

p_p & p_n represent the hole concentration in the P and N region respectively and n_p & n_n represent the electron concentration in the P and N region respectively.

At equilibrium, the minority carrier electron concentration in the P region n_p related to the majority carriers electron concentration N region n_n by the equation $n_p = n_n e^{-\frac{e}{kT}V_b}$

Applying some forward voltage the effective barrier potential decreases to $(V_b - V)$ hence some of the majority carriers diffuse across the junction. Thus holes diffuse to N-side and electrons to P-side. Consequently, minority carrier electron concentration at the edge of transition region on the P-side becomes greater than its equilibrium value by a small amount Δn_p. The majority carriers and electron concentration in the N region, however remain nearly constant.

Then $n_p + \Delta n_p = n_n e^{-\frac{e}{kT}(V_b - V)} = \left(n_p e^{\frac{e}{kT}V_b}\right)e^{-\frac{e}{kT}(V_b - V)} = n_p e^{\frac{e}{kT}V}$

Then $\Delta n_p = n_p\left(e^{\frac{e}{kT}V} - 1\right)$

Similarly, for excess holes on the N region $\Delta p_n = p_n\left(e^{\frac{e}{kT}V} - 1\right)$

The electron diffusion current injected into the P-region at the junction is given by

$$I_n = \frac{eAD_n}{L_n}\Delta n_p = \frac{eAD_n}{L_n} n_p \left(e^{\frac{e}{kT}V} - 1\right)$$

[Where A = area of cross-section of junction D_n = diffusion coefficient of electron

L_n = electron diffusion length]

Similarly, hole diffusion current injected into the N-region at the junction is given by$I_p =$

$\frac{eAD_p}{L_p}\Delta p_n = \frac{eAD_p}{L_p} p_n \left(e^{\frac{e}{kT}V} - 1\right)$

[Where D_p = diffusion coefficient of holes L_p = holes diffusion length]

The direction of both current is the same, the total diet current

$$I = I_n + I_p = \frac{eAD_n}{L_n} n_p \left(e^{\frac{e}{kT}V} - 1\right) + \frac{eAD_p}{L_p} p_n \left(e^{\frac{e}{kT}V} - 1\right)$$

$$= eA\left\{\frac{D_n}{L_n} n_p + \frac{D_p}{L_p} p_n\right\}\left(e^{\frac{e}{kT}V} - 1\right)$$

$$= I_0 \left(e^{\frac{eV}{kT}} - 1\right) \ldots\ldots\ldots\ldots\ldots\text{(i)} \qquad \left[\text{Where } I_0 = eA\left\{\frac{D_n}{L_n} n_p + \frac{D_p}{L_p} p_n\right\}\right]$$

The empirical form of the equation (i) is $I_0 \left(e^{\frac{eV}{\eta kT}} - 1\right)$ where η is a numerical constant

which depends up on metro of the diode for Ge $\eta = 1$ but Si $\eta = 2$

(****) It is not included in the revised syllabus